

Silicon PNP Power Transistors**2SA769****DESCRIPTION**

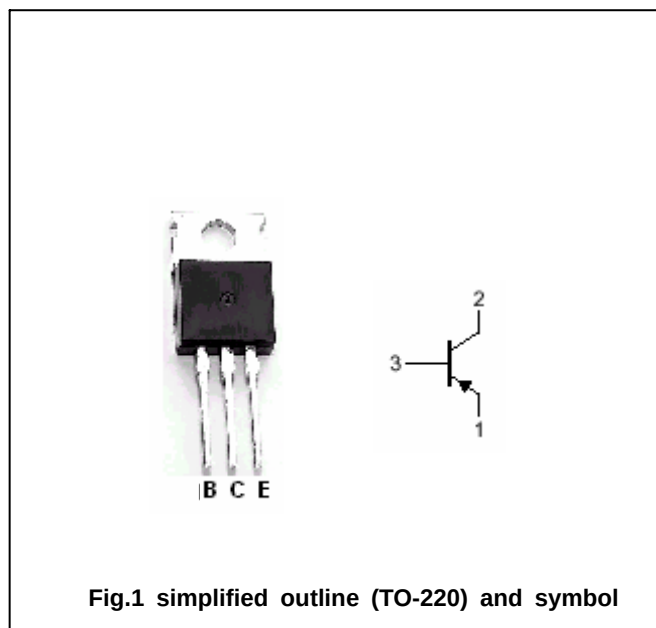
- With TO-220 package
- Complement to type 2SC1827

APPLICATIONS

- For low frequency power amplifier applications

PINNING

PIN	DESCRIPTION
1	Emitter
2	Collector;connected to mounting base
3	Base

**Absolute maximum ratings(Ta=25°C)**

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
V_{CBO}	Collector-base voltage	Open emitter	-80	V
V_{CEO}	Collector-emitter voltage	Open base	-80	V
V_{EBO}	Emitter-base voltage	Open collector	-5	V
I_C	Collector current		-4	A
P_C	Collector power dissipation	$T_C=25^{\circ}\text{C}$	30	W
T_j	Junction temperature		150	$^{\circ}\text{C}$
T_{stg}	Storage temperature		-55~150	$^{\circ}\text{C}$

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CHARACTERISTICS

T_j=25°C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT
V _{(BR)CEO}	Collector-emitter breakdown voltage	I _C =-25mA, I _B =0	-80			V
V _{(BR)CBO}	Collector-base breakdown voltage	I _C =-1mA, I _E =0	-80			V
V _{CEsat}	Collector-emitter saturation voltage	I _C =-3A; I _B =-0.3A			-1.0	V
V _{BEsat}	Base-emitter saturation voltage	I _C =-3A; I _B =-0.3A			-1.5	V
I _{CBO}	Collector cut-off current	V _{CB} =-80V; I _E =0			-10	μA
I _{EBO}	Emitter cut-off current	V _{EB} =-5V; I _C =0			-10	μA
h _{FE}	DC current gain	I _C =-1A; V _{CE} =-4V	60		240	
f _T	Transition frequency	I _C =-0.5A; V _{CE} =-10V		10		MHz

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PACKAGE OUTLINE

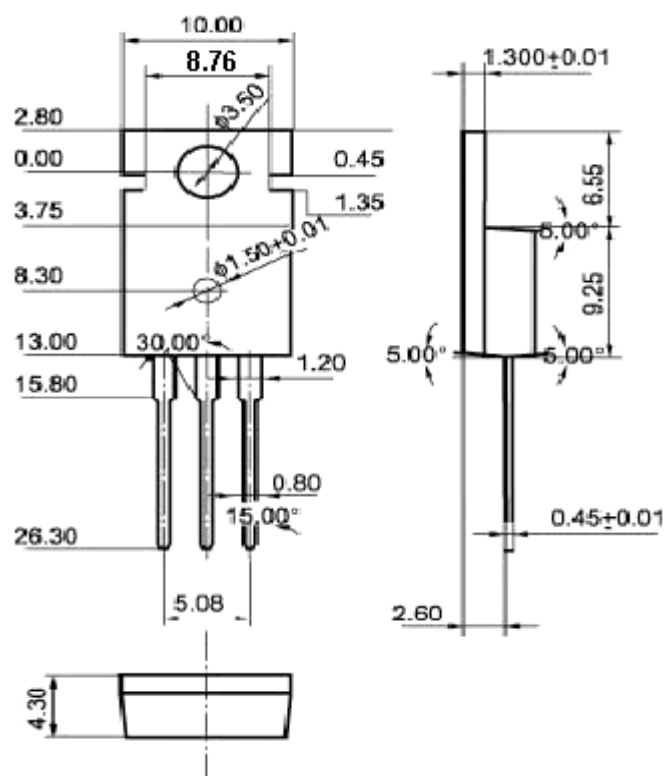


Fig.2 Outline dimensions(unindicated tolerance:±0.10 mm)