

Silicon PNP Power Transistors

2SB1063

DESCRIPTION

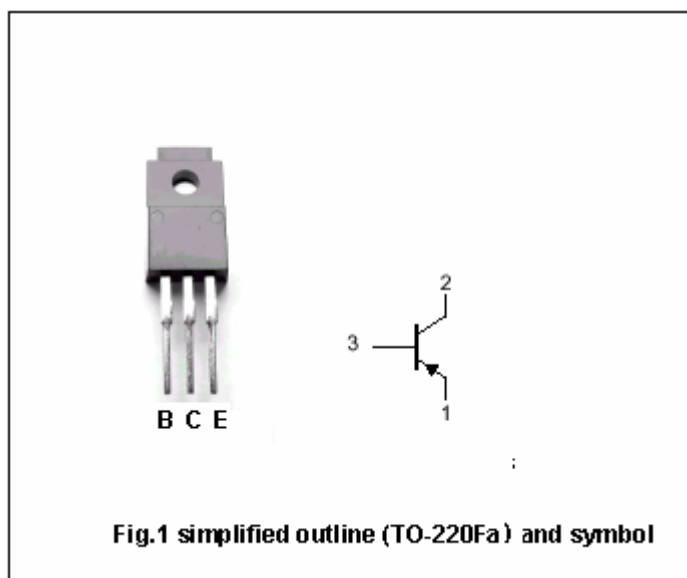
- With TO-220Fa package
- Complement to type 2SD1499
- Wide area of safe operation
- High f_T

APPLICATIONS

- For high power amplifier applications

PINNING

PIN	DESCRIPTION
1	Emitter
2	Collector
3	Base

Absolute maximum ratings($T_a=25^\circ\text{C}$)

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
V_{CBO}	Collector-base voltage	Open emitter	-100	V
V_{CEO}	Collector -emitter voltage	Open base	-100	V
V_{EBO}	Emitter-base voltage	Open collector	-5	V
I_C	Collector current		-5	A
I_{CM}	Collector current-peak		-8	A
P_C	Collector power dissipation	$T_a=25$	2.0	W
		$T_C=25$	40	
T_j	Junction temperature		150	
T_{stg}	Storage temperature		-55~150	

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CHARACTERISTICS

T_j=25 unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT
V _{CEsat}	Collector-emitter saturation voltage	I _C =-3A ; I _B =-0.3A			-2.0	V
V _{BE}	Base-emitter on voltage	I _C =-3A ; V _{CE} =-5V			-1.8	V
I _{CBO}	Collector cut-off current	V _{CB} =-100V; I _E =0			-50	μ A
I _{EBO}	Emitter cut-off current	V _{EB} =-3V; I _C =0			-50	μ A
h _{FE-1}	DC current gain	I _C =-20mA ; V _{CE} =-5V	20			
h _{FE-2}	DC current gain	I _C =-1A ; V _{CE} =-5V	40		200	
h _{FE-3}	DC current gain	I _C =-3A ; V _{CE} =-5V	20			
f _T	Transition frequency	I _C =-0.5A ; V _{CE} =-5V		20		MHz
C _{OB}	Collector output capacitance	I _E =0 ; V _{CB} =-10V; f=1MHz		170		pF

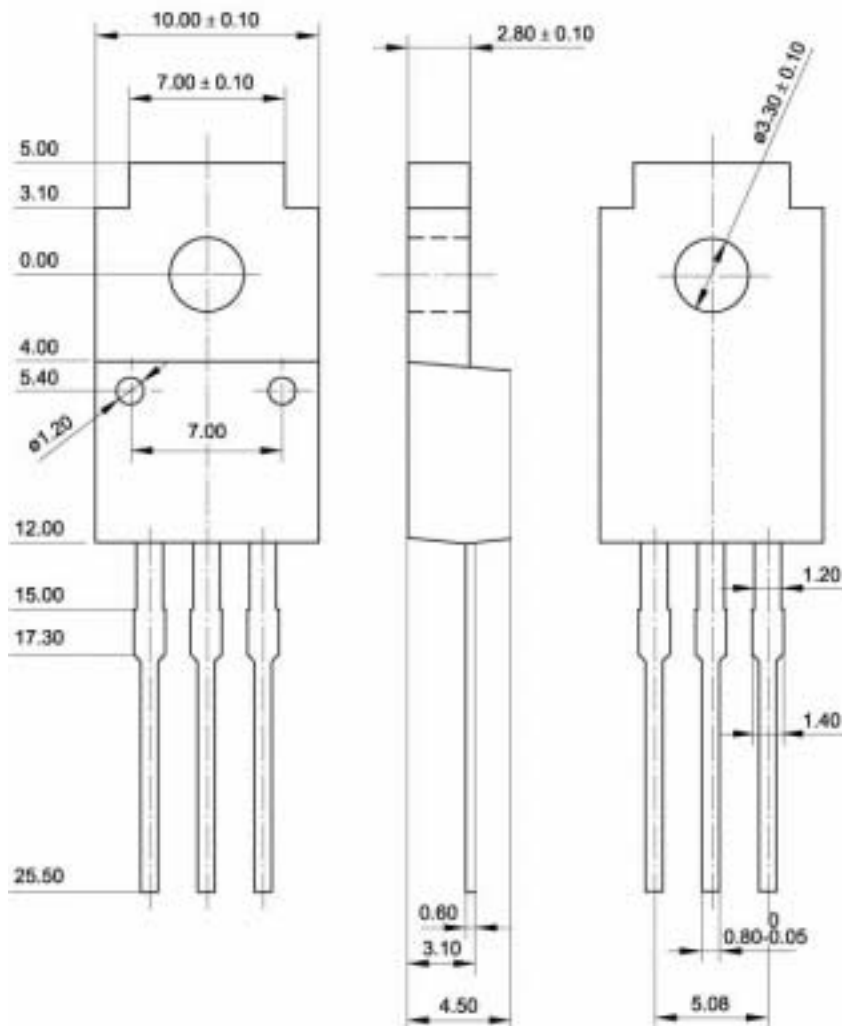
◆ h_{FE-2} Classifications

R	Q	P
40-80	60-120	100-200

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PACKAGE OUTLINE

Fig.2 Outline dimensions (unindicated tolerance: ± 0.15 mm)