

Silicon PNP Power Transistors

2SB554

DESCRIPTION

- With TO-3 package
- Complement to type 2SD424
- High power dissipation

APPLICATIONS

- For use in power amplifier applications

PINNING(see Fig.2)

PIN	DESCRIPTION
1	Base
2	Emitter
3	Collector

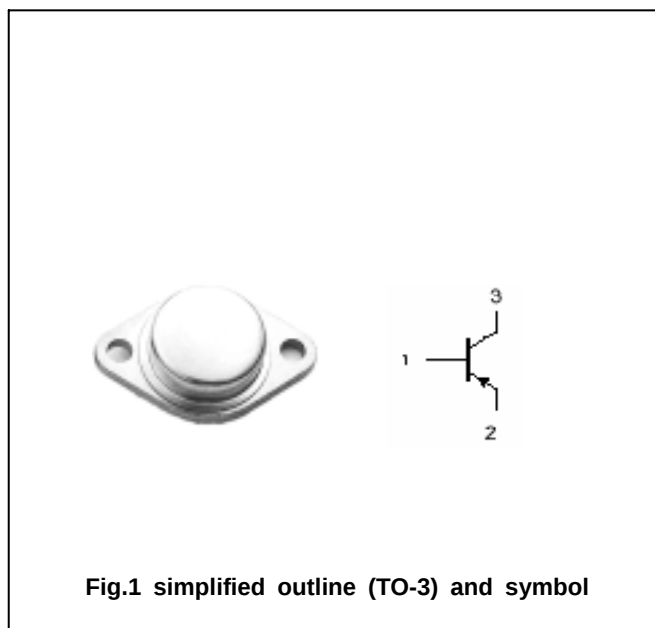


Fig.1 simplified outline (TO-3) and symbol

Absolute maximum ratings($T_a =$)

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
V_{CBO}	Collector-base voltage	Open emitter	-180	V
V_{CEO}	Collector-emitter voltage	Open base	-180	V
V_{EBO}	Emitter-base voltage	Open collector	-5	V
I_C	Collector current		-15	A
I_B	Base current		-4	A
P_C	Collector power dissipation	$T_C = 25$	150	W
T_j	Junction temperature		150	
T_{stg}	Storage temperature		-55~200	

Silicon PNP Power Transistors

2SB554

CHARACTERISTICS

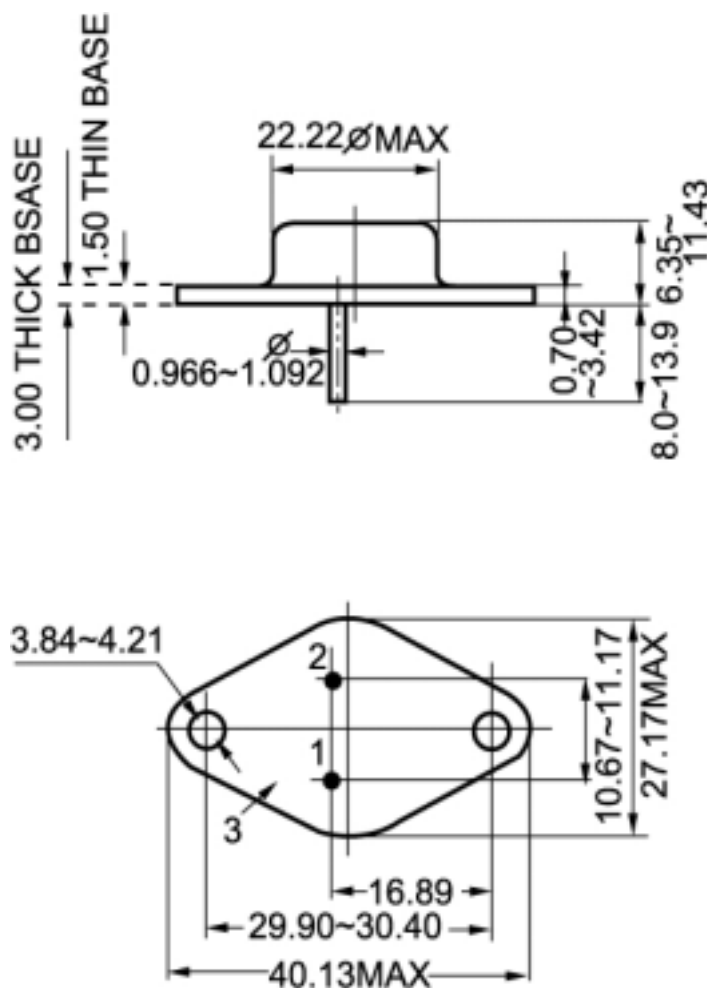
T_j=25 unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT
V _{(BR)CEO}	Collector-emitter breakdown voltage	I _C =-25mA ; I _B =0	-180			V
V _{CEsat}	Collector-emitter saturation voltage	I _C =-10A; I _B =-1A			-3.0	V
V _{BE}	Base-emitter on voltage	I _C =-2A ; V _{CE} =-5V			-1.5	V
I _{CBO}	Collector cut-off current	V _{CB} =-90V; I _E =0			-0.1	mA
I _{EBO}	Emitter cut-off current	V _{EB} =-5V; I _C =0			-0.1	mA
h _{FE}	DC current gain	I _C =-2A ; V _{CE} =-5V	40		140	
C _{OB}	Output capacitance	I _E =0 ; V _{CB} =-10V; f=1.0MHz		450		pF
f _T	Transition frequency	I _C =-2A ; V _{CE} =-5V		6		MHz

Silicon PNP Power Transistors

2SB554

PACKAGE OUTLINE

Fig.2 outline dimensions (unindicated tolerance: $\pm 0.1\text{mm}$)