

DATA SHEET

BF1105; BF1105R; BF1105WR N-channel dual-gate MOS-FETs

Product specification
Supersedes data of 1997 Dec 01
File under Discrete Semiconductors, SC07

1997 Dec 02

N-channel dual-gate MOS-FETs

BF1105; BF1105R; BF1105WR

FEATURES

- Short channel transistor with high forward transfer admittance to input capacitance ratio
- Low noise gain controlled amplifier up to 1 GHz.
- Internal self-biasing circuit to ensure good cross-modulation performance during AGC and good DC stabilization.

APPLICATIONS

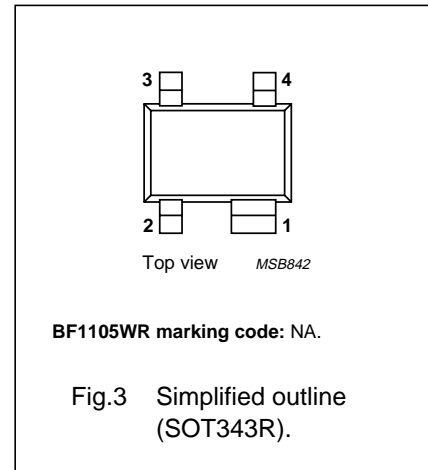
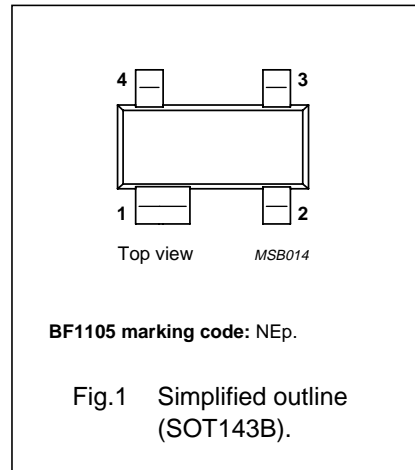
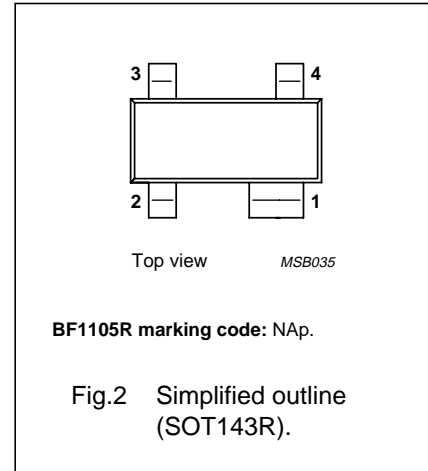
- VHF and UHF applications with 5 V supply voltage, such as television tuners and professional communications equipment.

DESCRIPTION

Enhancement type N-channel field-effect transistor with source and substrate interconnected. Integrated diodes between gates and source protect against excessive input voltage surges. The BF1105, BF1105R and BF1105WR are encapsulated in the SOT143B, SOT143R and SOT343R plastic packages respectively.

PINNING

PIN	DESCRIPTION
1	source
2	drain
3	gate 2
4	gate 1



QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DS}	drain-source voltage		–	–	7	V
I_D	drain current		–	–	30	mA
P_{tot}	total power dissipation	$T_{amb} \leq 80^\circ C$	–	–	200	mW
$ y_{fs} $	forward transfer admittance		25	31	–	mS
C_{ig1-ss}	input capacitance at gate 1		–	2.2	2.7	pF
C_{rss}	reverse transfer capacitance	$f = 1\text{ MHz}$	–	25	40	fF
F	noise figure	$f = 800\text{ MHz}$	–	1.7	2.5	dB
X_{mod}	cross-modulation	input level for $k = 1\%$ at 40 dB AGC	100	–	–	dB μ V
T_j	operating junction temperature		–	–	150	$^\circ C$

CAUTION

This product is supplied in anti-static packing to prevent damage caused by electrostatic discharge during transport and handling. For further information, refer to Philips specs.: SNW-EQ-608, SNW-FQ-302A and SNW-FQ-302B.

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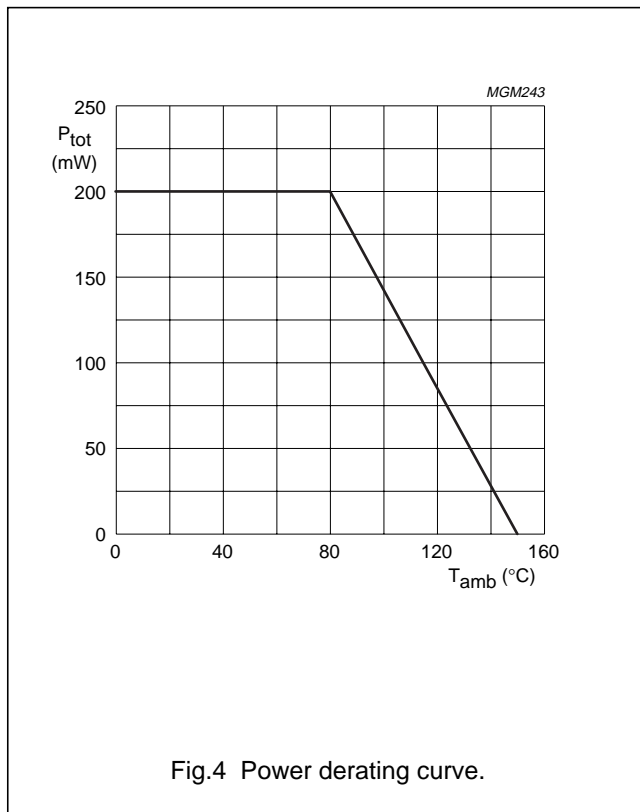
LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V _{DS}	drain-source voltage		–	7	V
I _D	drain current		–	30	mA
I _{G1}	gate 1 current		–	±10	mA
I _{G2}	gate 2 current		–	±10	mA
P _{tot}	total power dissipation	T _{amb} ≤ 80 °C; note 1; see Fig.4	–	200	mW
T _{stg}	storage temperature		–65	+150	°C
T _j	operating junction temperature		–	+150	°C

Note

1. Device mounted on a printed-circuit board.



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THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j-a}$	thermal resistance from junction to ambient in free air	note 1	350	K/W
$R_{th\ j-s}$	thermal resistance from junction to soldering point		200	K/W

Note

1. Device mounted on a printed-circuit board.

STATIC CHARACTERISTICS

$T_j = 25\text{ °C}$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{G1-S} = V_{G2-S} = 0$; $I_D = 10\ \mu A$	7	–	–	V
$V_{(BR)G1-SS}$	gate 1-source breakdown voltage	$V_{G2-S} = 0$; $I_D = 0$; $I_{G1-S} = 10\ \mu A$	7	–	–	V
$V_{(BR)G2-SS}$	gate 2-source breakdown voltage	$V_{G1-S} = V_{DS} = 0$; $I_{G2-S} = 10\ \mu A$	7	–	–	V
$V_{G2-S(th)}$	gate 2-source threshold voltage	$V_{G1-S} = 5\ V$; $V_{DS} = 5\ V$; $I_D = 20\ \mu A$	0.3	0.8	1.2	V
I_{DSX}	self-biasing drain current	$V_{G2-S} = 4\ V$; $V_{DS} = 5\ V$	8	–	16	mA
I_{G1-SS}	gate 1 cut-off current	$V_{G1-S} = 5\ V$; $V_{G2-S} = 0$; $I_D = 0$	–	–	50	nA
I_{G2-SS}	gate 2 cut-off current	$V_{G1-S} = V_{DS} = 0$; $V_{G2-S} = 4\ V$	–	–	20	nA

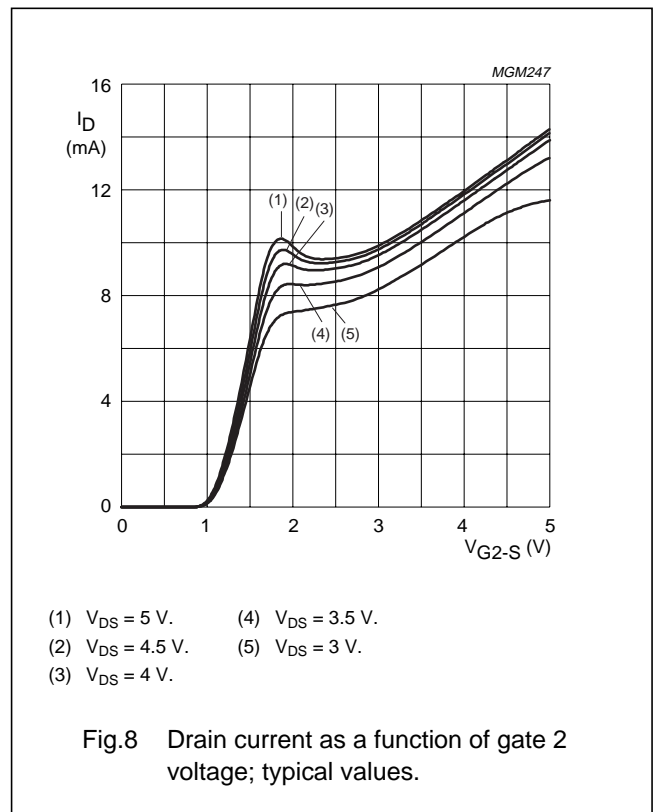
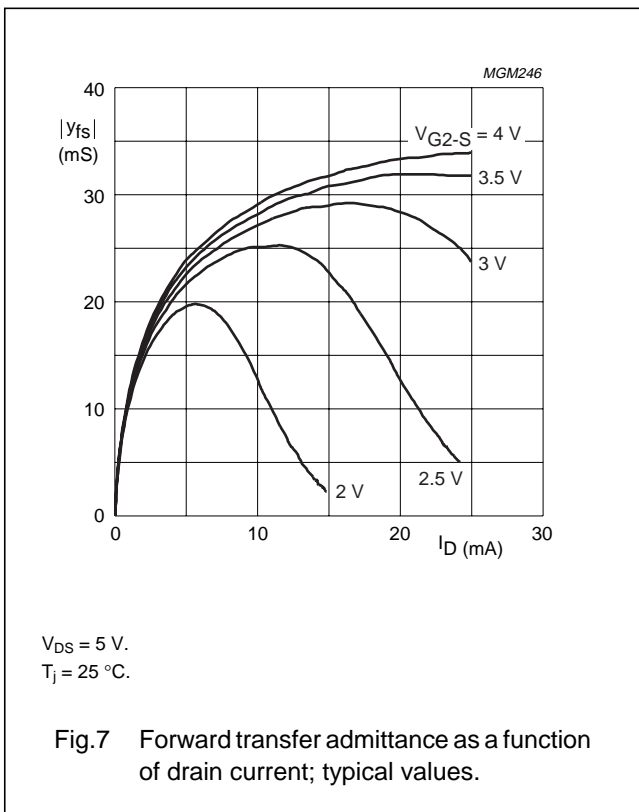
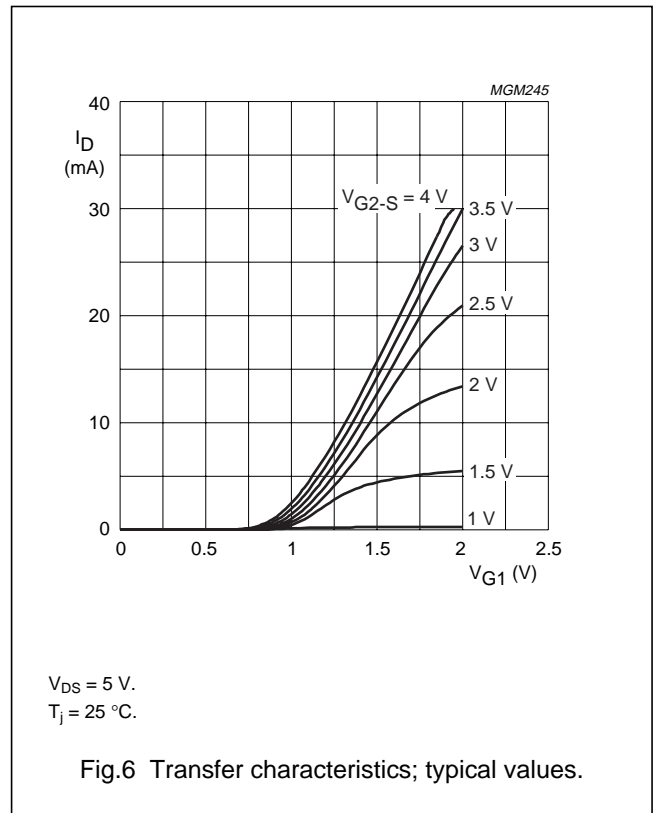
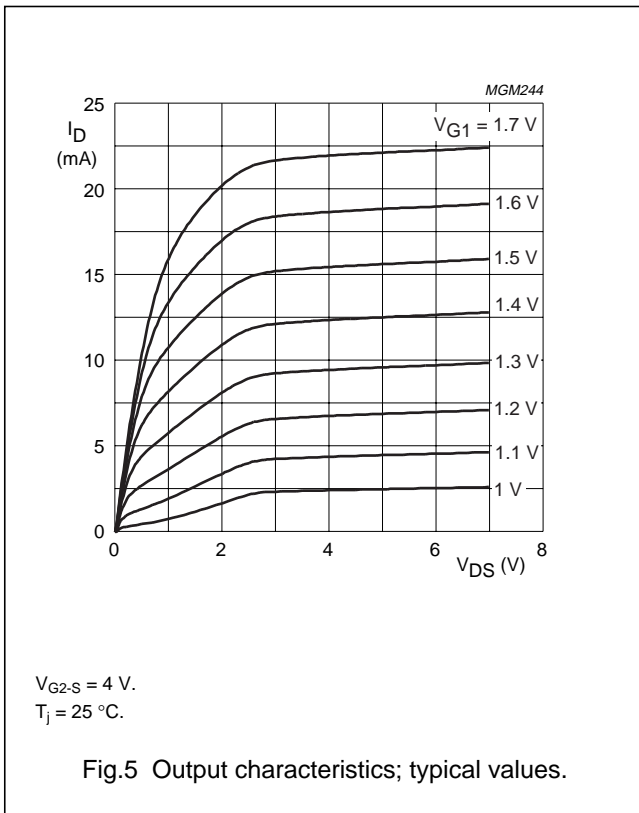
DYNAMIC CHARACTERISTICS

Common source; $T_{amb} = 25\text{ °C}$; $V_{G2-S} = 4\ V$; $V_{DS} = 5\ V$; self-biasing current; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$ y_{fs} $	forward transfer admittance	pulsed; $T_j = 25\text{ °C}$	25	31	–	mS
C_{ig1-ss}	input capacitance at gate 1	$f = 1\ \text{MHz}$	–	2.2	2.7	pF
C_{ig2-ss}	input capacitance at gate 2	$f = 1\ \text{MHz}$	–	1.6	–	pF
C_{oss}	output capacitance	$f = 1\ \text{MHz}$	–	1.2	–	pF
C_{rss}	reverse transfer capacitance	$f = 1\ \text{MHz}$	–	25	40	fF
F	noise figure	$f = 800\ \text{MHz}$; $Y_S = Y_{S\ opt}$	–	1.7	2.5	dB
G_p	power gain	$G_S = 2\ \text{mS}$; $B_S = B_{S\ opt}$; $G_L = 0.5\ \text{mS}$; $B_L = B_{L\ opt}$; $f = 200\ \text{MHz}$; see Fig.16	–	38	–	dB
		$G_S = 3.3\ \text{mS}$; $B_S = B_{S\ opt}$; $G_L = 1\ \text{mS}$; $B_L = B_{L\ opt}$; $f = 800\ \text{MHz}$; see Fig.17	–	20	–	dB
X_{mod}	cross-modulation	input level for $k = 1\%$ at 0 dB AGC; $f_w = 50\ \text{MHz}$; $f_{unw} = 60\ \text{MHz}$; see Fig.18	85	–	–	dB μ V
		input level for $k = 1\%$ at 40 dB AGC; $f_w = 50\ \text{MHz}$; $f_{unw} = 60\ \text{MHz}$; see Fig.18	100	–	–	dB μ V

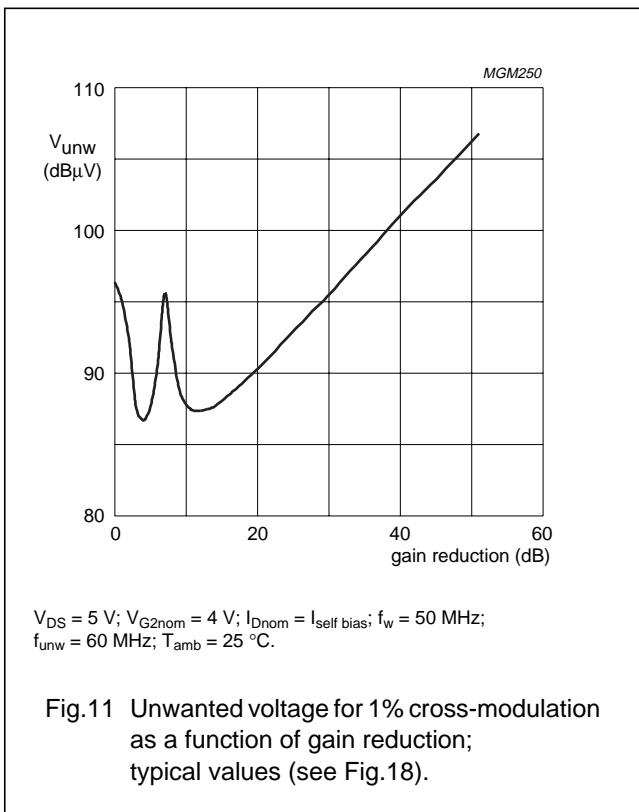
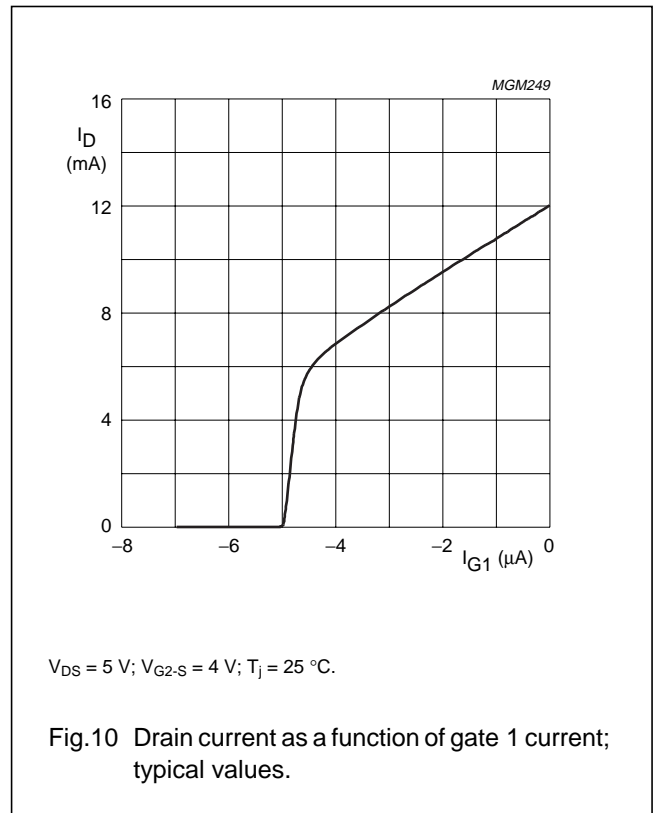
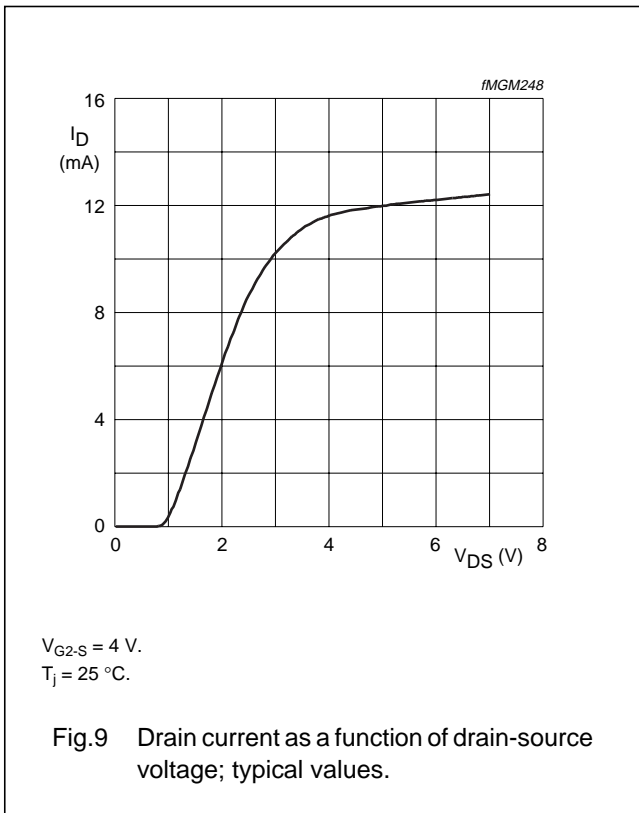
N-channel dual-gate MOS-FETs

BF1105; BF1105R; BF1105WR



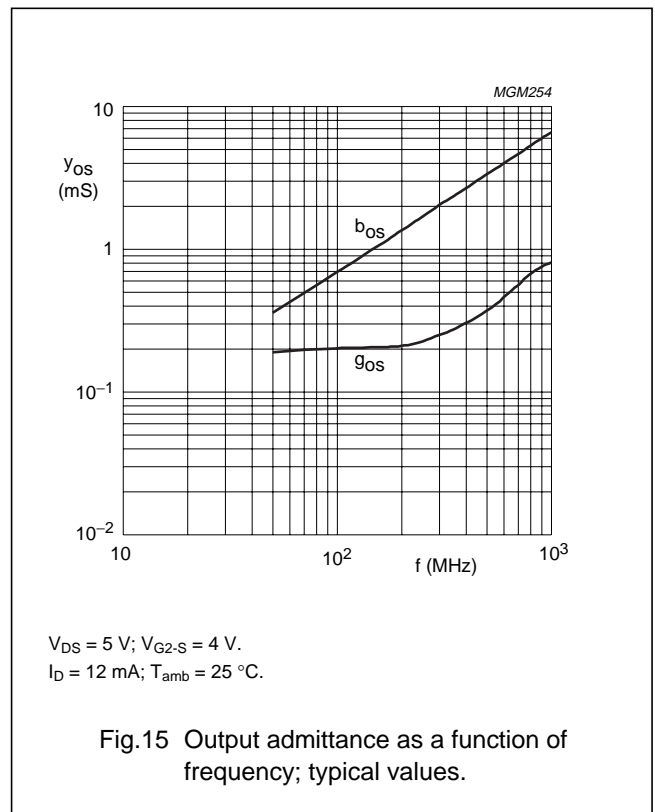
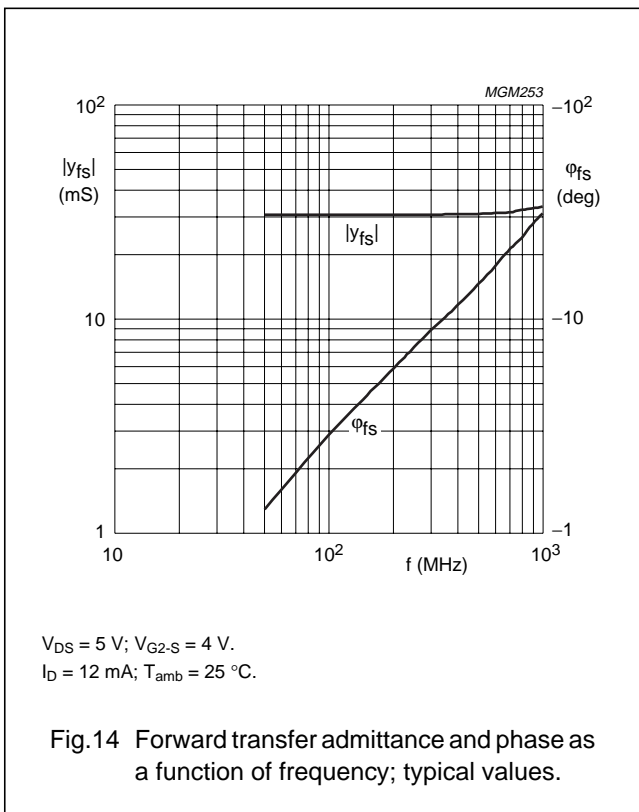
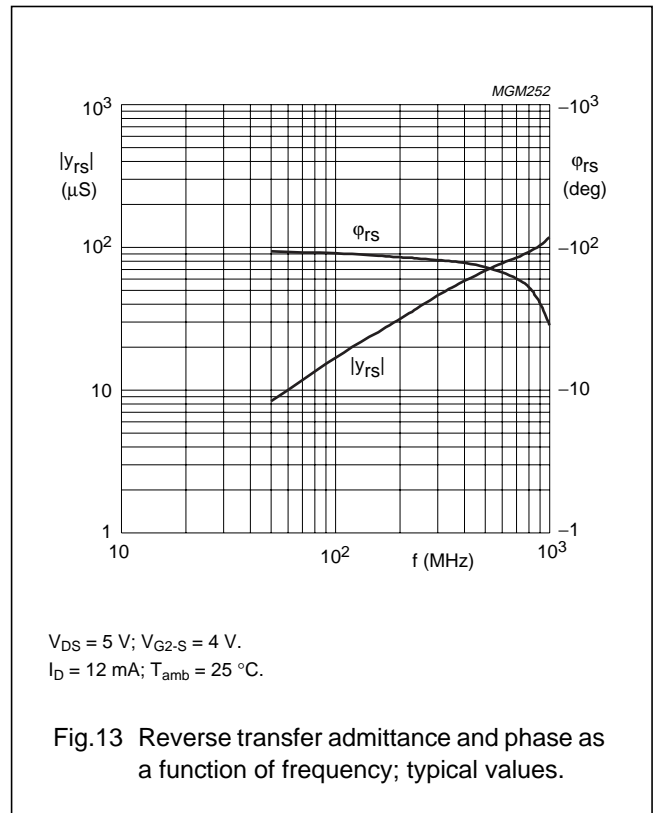
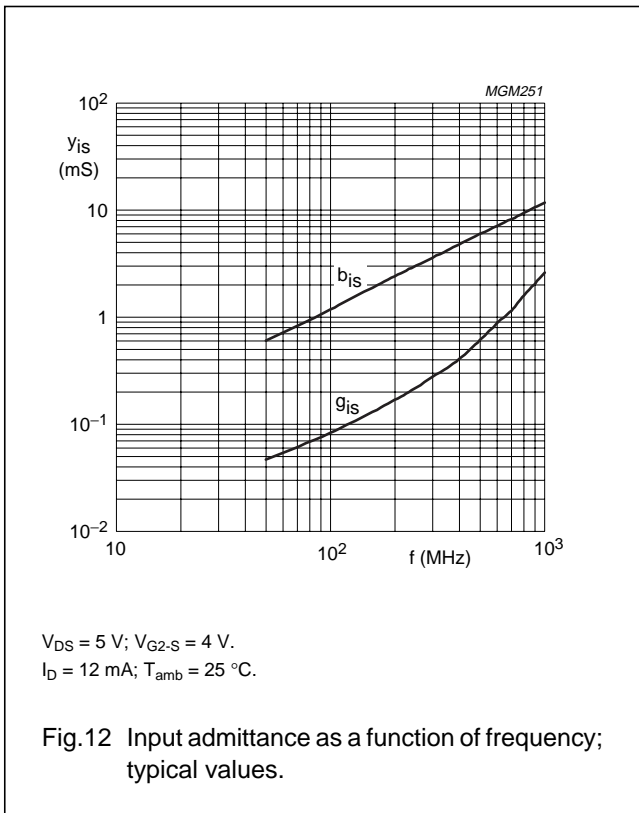
N-channel dual-gate MOS-FETs

BF1105; BF1105R; BF1105WR



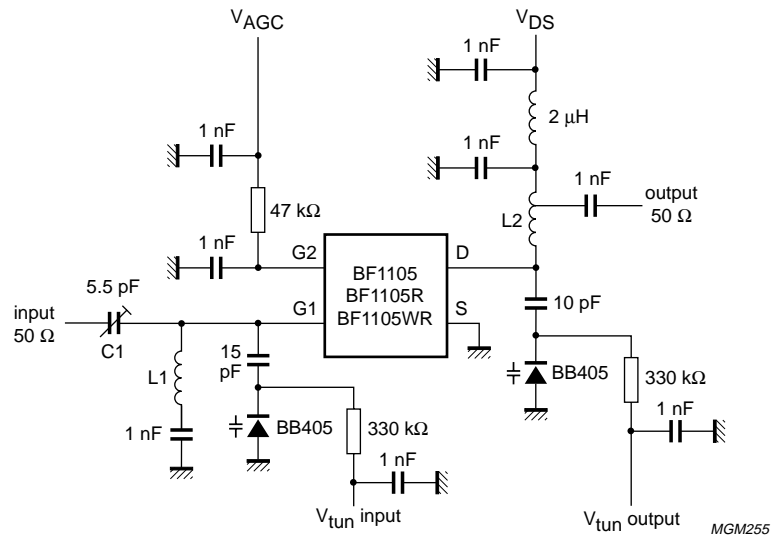
N-channel dual-gate MOS-FETs

BF1105; BF1105R; BF1105WR



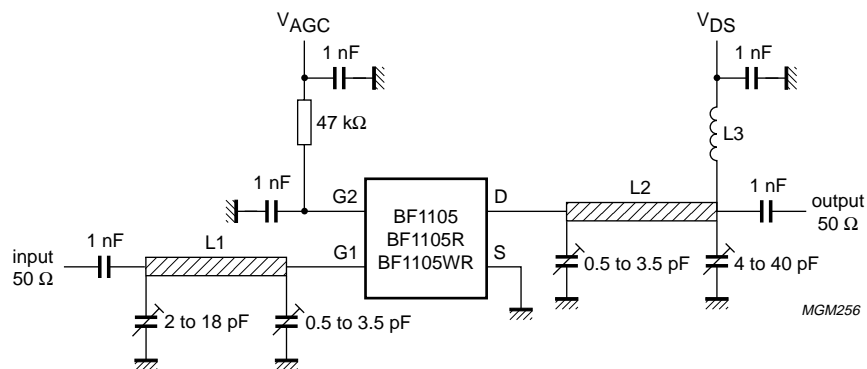
N-channel dual-gate MOS-FETs

BF1105; BF1105R; BF1105WR



$V_{DS} = 5\text{ V}$, $G_S = 2\text{ mS}$, $G_L = 0.5\text{ mS}$, $f = 200\text{ MHz}$.
 $L1 = 45\text{ nH}$, 4 turns, internal diameter = 4 mm, 0.8 mm copper wire.
 $L2 = 160\text{ nH}$, 3 turns, internal diameter = 8 mm, 0.8 mm copper wire; tapped at approximately half a turn from the cold side, to set $G_L = 0.5\text{ mS}$.
 $C1$ adjusted for $G_S = 2\text{ mS}$.

Fig.16 Gain test circuit.



$V_{DS} = 5\text{ V}$, $G_S = 3.3\text{ mS}$, $G_L = 1\text{ mS}$, $f = 800\text{ MHz}$.
 $L1 = 2\text{ cm}$, silvered 0.8 mm copper wire 4 mm above ground plane.
 $L2 = 2\text{ cm}$, silvered 0.8 mm copper wire 4 mm above ground plane.
 $L3 = 11\text{ turns}$ 0.5 mm copper wire without spacing, internal diameter = 3 mm, $L = \text{approx. } 200\text{ nH}$.

Fig.17 Gain test circuit.

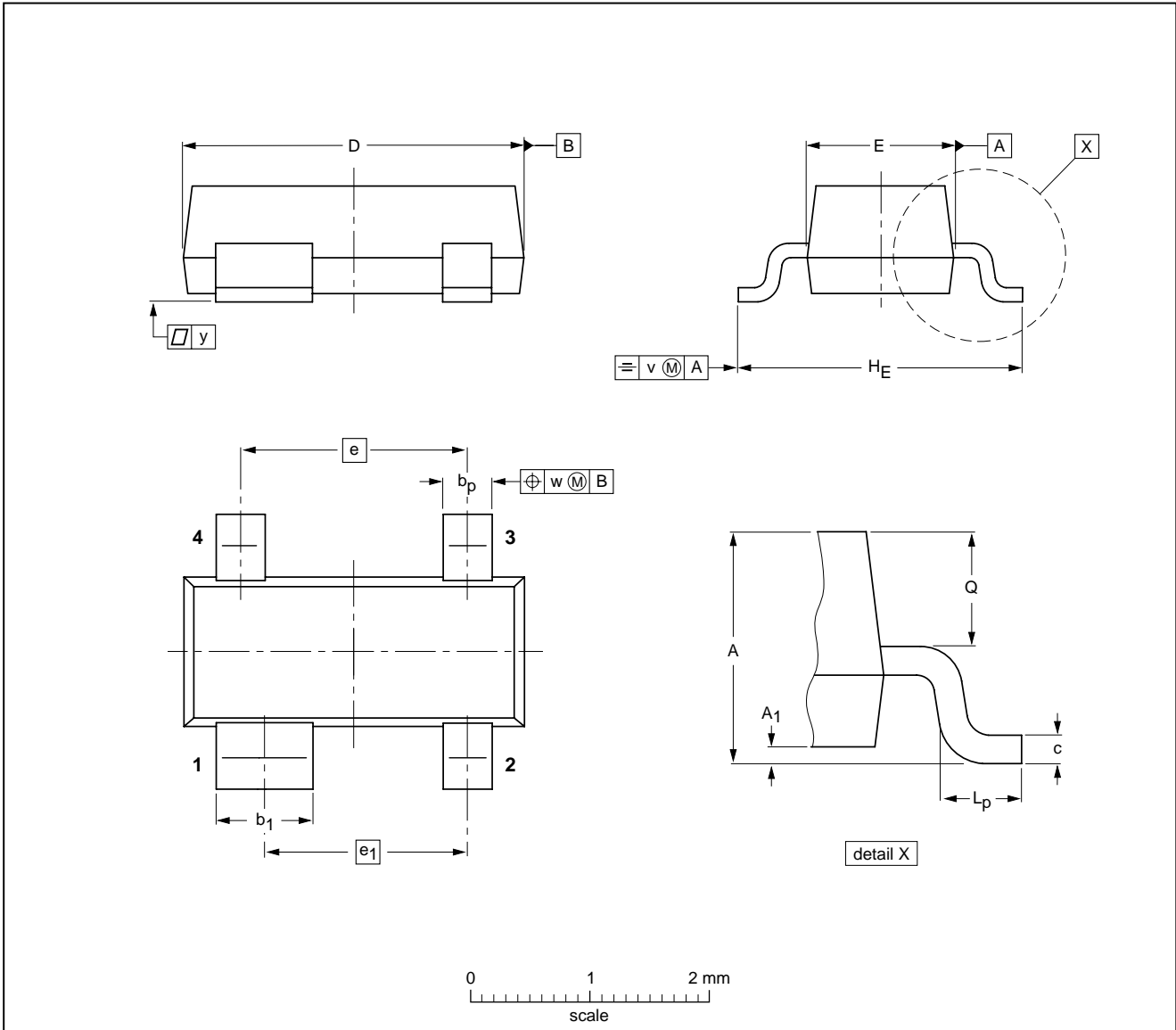
N-channel dual-gate MOS-FETs

BF1105; BF1105R; BF1105WR

PACKAGE OUTLINES

Plastic surface mounted package; 4 leads

SOT143B



DIMENSIONS (mm are the original dimensions)

UNIT	A	A ₁ max	b _p	b ₁	c	D	E	e	e ₁	H _E	L _p	Q	v	w	y
mm	1.1 0.9	0.1	0.48 0.38	0.88 0.78	0.15 0.09	3.0 2.8	1.4 1.2	1.9	1.7	2.5 2.1	0.45 0.15	0.55 0.45	0.2	0.1	0.1

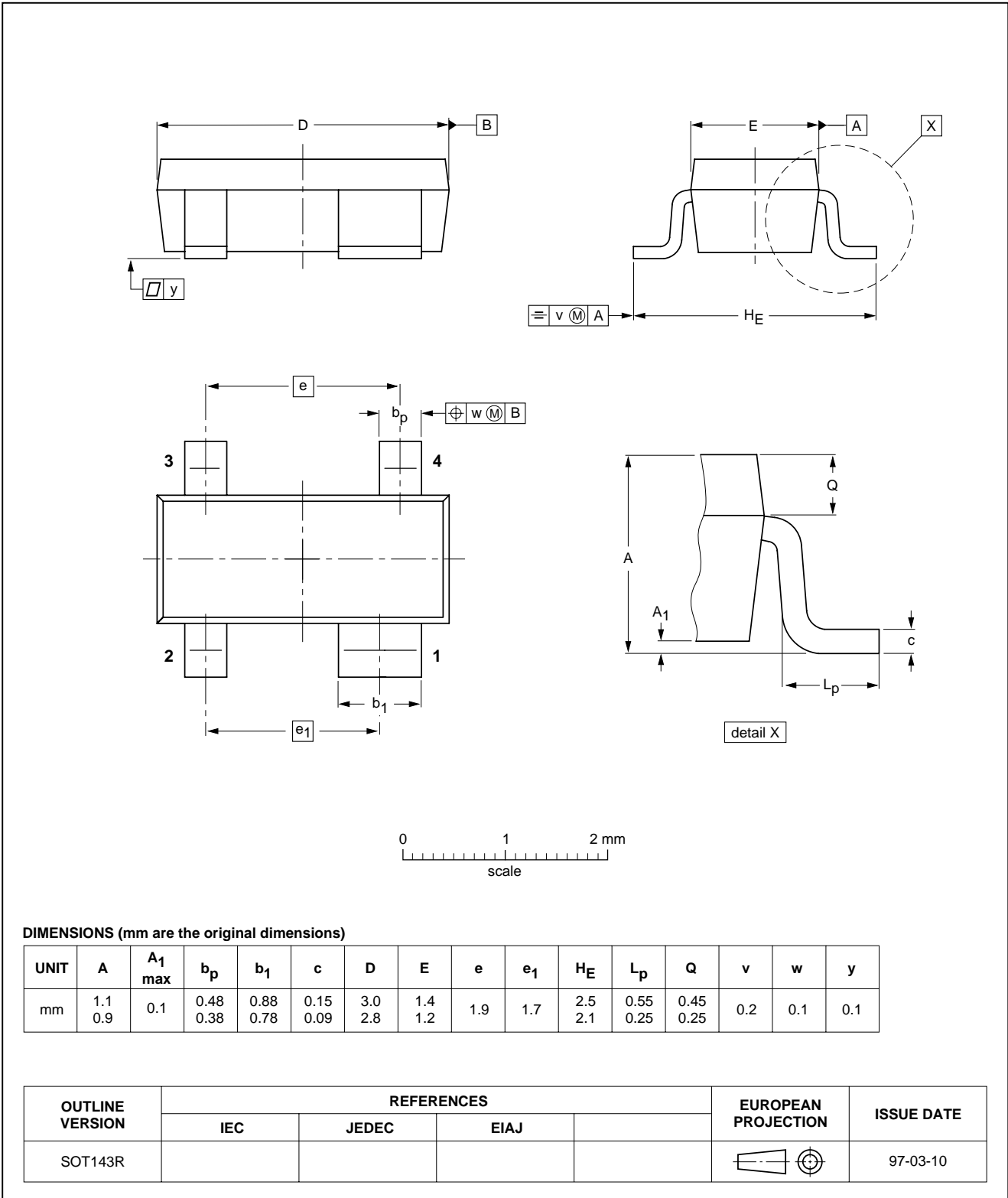
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	IEC	JEDEC	EIAJ			
SOT143B						97-02-28

N-channel dual-gate MOS-FETs

BF1105; BF1105R; BF1105WR

Plastic surface mounted package; reverse pinning; 4 leads

SOT143R

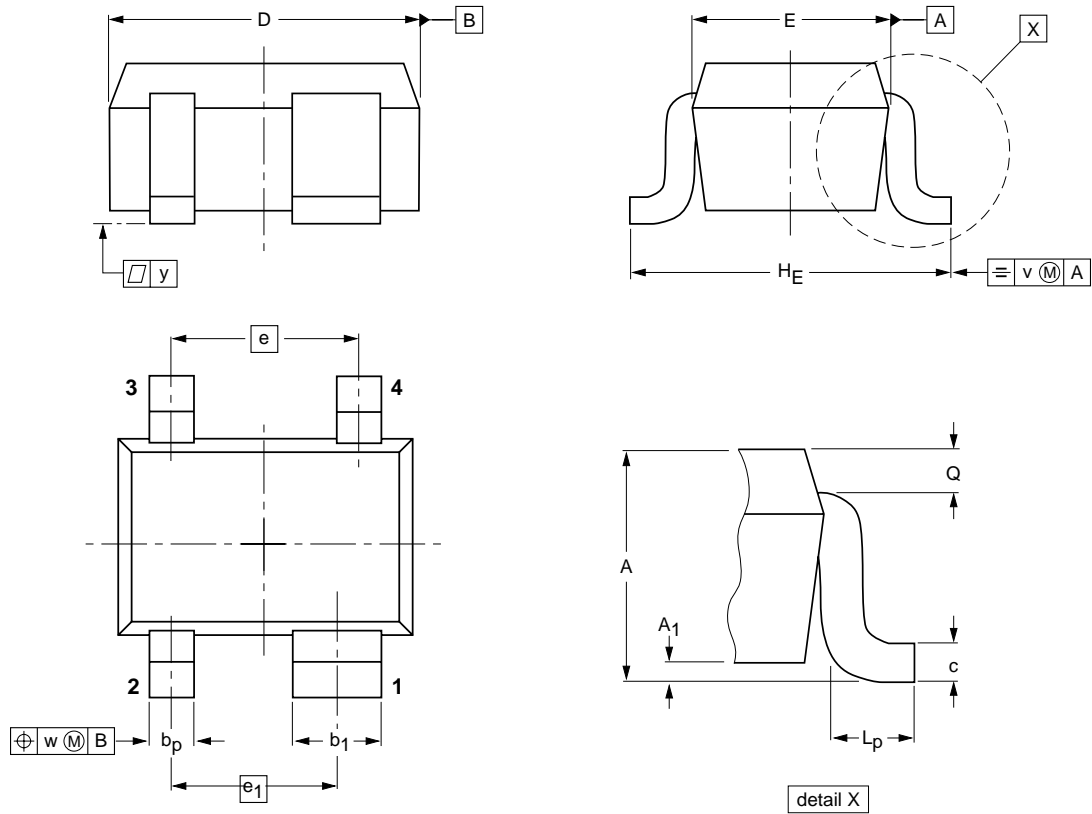


N-channel dual-gate MOS-FETs

BF1105; BF1105R; BF1105WR

Plastic surface mounted package; reverse pinning; 4 leads

SOT343R



DIMENSIONS (mm are the original dimensions)

UNIT	A	A ₁ max	b _p	b ₁	c	D	E	e	e ₁	H _E	L _p	Q	v	w	y
mm	1.1 0.8	0.1	0.4 0.3	0.7 0.5	0.25 0.10	2.2 1.8	1.35 1.15	1.3	1.15	2.2 2.0	0.45 0.15	0.23 0.13	0.2	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT343R						97-05-21

N-channel dual-gate MOS-FETs

BF1105; BF1105R; BF1105WR

DEFINITIONS

Data Sheet Status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

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NOTES

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BF1105; BF1105R; BF1105WR

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